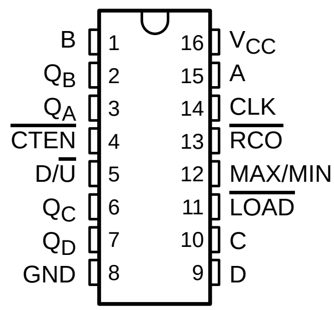
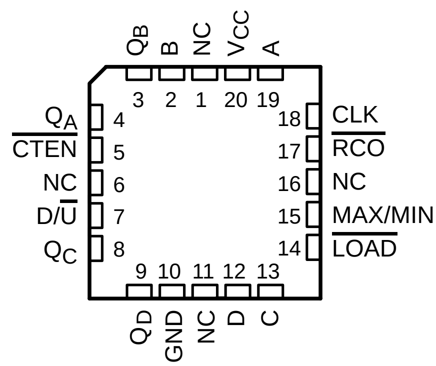
- **Wide Operating Voltage Range of 2 V to 6 V**
- **Outputs Can Drive Up To 10 LSTTL Loads**
- **Low Power Consumption, 80-µA Max I_{CC}**
- **Typical t_{pd} = 13 ns**
- **±4-mA Output Drive at 5 V**
- **Low Input Current of 1 µA Max**
- **Single Down/Up Count-Control Line**
- **Look-Ahead Circuitry Enhances Speed of Cascaded Counters**
- **Fully Synchronous in Count Modes**
- **Asynchronously Presettable With Load Control**

SN54HC191 . . . J OR W PACKAGE
SN74HC191 . . . D, N, OR NS PACKAGE
(TOP VIEW)



SN54HC191 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The ’HC191 devices are 4-bit synchronous, reversible, up/down binary counters. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

The outputs of the four flip-flops are triggered on a low- to high-level transition of the clock (CLK) input if the count-enable ($\overline{\text{CTEN}}$) input is low. A high at $\overline{\text{CTEN}}$ inhibits counting. The direction of the count is determined by the level of the down/up (D/$\overline{\text{U}}$) input. When D/$\overline{\text{U}}$ is low, the counter counts up, and when D/$\overline{\text{U}}$ is high, it counts down.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube	SN74HC191N	SN74HC191N
	SOIC – D	Tube	SN74HC191D	HC191
		Tape and reel	SN74HC191DR	
	SOP – NS	Tape and reel	SN74HC191NSR	HC191
–55°C to 125°C	CDIP – J	Tube	SNJ54HC191J	SNJ54HC191J
	CFP – W	Tube	SNJ54HC191W	SNJ54HC191W
	LCCC – FK	Tube	SNJ54HC191FK	SNJ54HC191FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

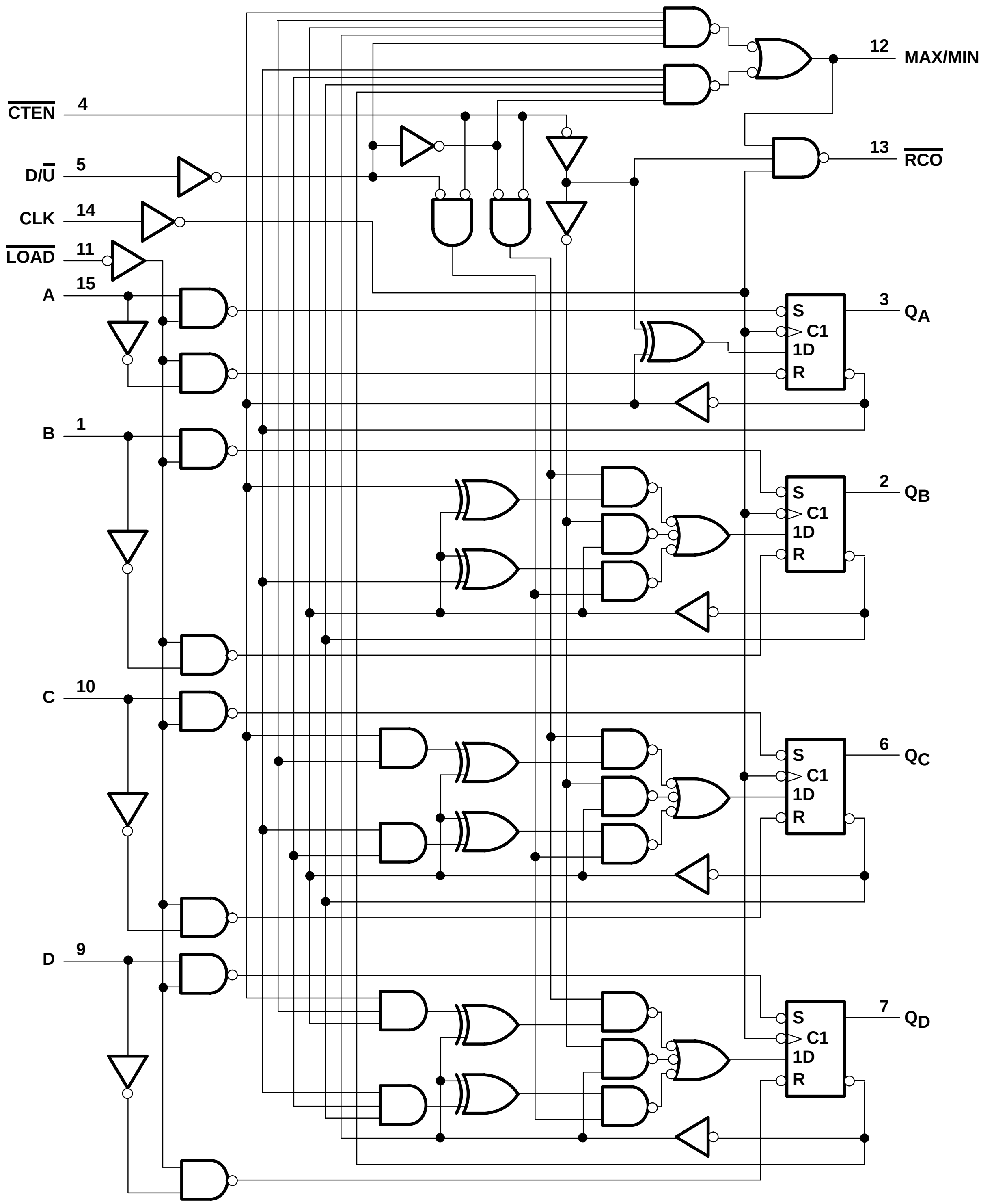
description/ordering information (continued)

These counters feature a fully independent clock circuit. Change at the control ($\overline{\text{CTEN}}$ and D/$\overline{\text{U}}$) inputs that modifies the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter is dictated solely by the condition meeting the stable setup and hold times.

These counters are fully programmable; that is, each of the outputs can be preset to either level by placing a low on the load ($\overline{\text{LOAD}}$) input and entering the desired data at the data inputs. The output changes to agree with the data inputs independently of the level of CLK. This feature allows the counters to be used as modulo-N dividers simply by modifying the count length with the preset inputs.

Two outputs are available to perform the cascading function: ripple clock ($\overline{\text{RCO}}$) and maximum/minimum (MAX/MIN) count. MAX/MIN produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down, or maximum (9 or 15) counting up. $\overline{\text{RCO}}$ produces a low-level output pulse under those same conditions, but only while CLK is low. The counters can be cascaded easily by feeding $\overline{\text{RCO}}$ to $\overline{\text{CTEN}}$ of the succeeding counter if parallel clocking is used, or to CLK if parallel enabling is used. MAX/MIN can be used to accomplish look ahead for high-speed operation.

logic diagram (positive logic)

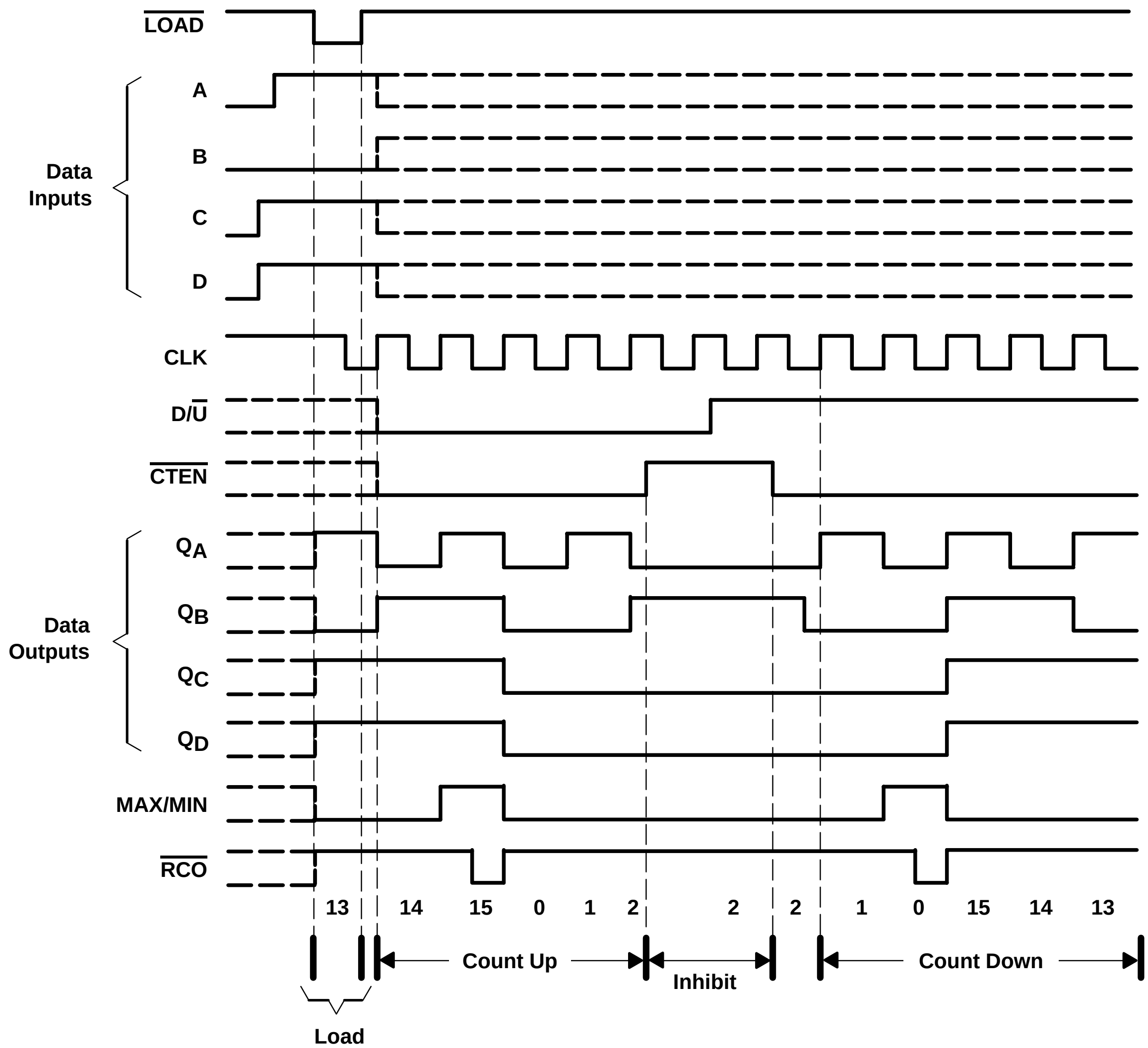


Pin numbers shown are for the D, J, N, NS, and W packages.

typical load, count, and inhibit sequence

The following sequence is illustrated below:

1. Load (preset) to binary 13
2. Count up to 14, 15 (maximum), 0, 1, and 2
3. Inhibit
4. Count down to 1, 0 (minimum), 15, 14, and 13



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	73°C/W
N package	67°C/W
NS package	64°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			SN54HC191			SN74HC191			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.5			0.5	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 6 V			1.8			1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$‡	Input transition rise/fall time	V_{CC} = 2 V			1000			1000	ns
		V_{CC} = 4.5 V			500			500	
		V_{CC} = 6 V			400			400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

‡ If this device is used in the threshold region (from V_{IL}max = 0.5 V to V_{IH}min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t_t = 1000 ns and V_{CC} = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C MIN	TYP	MAX	SN54HC191 MIN	MAX	SN74HC191 MIN	MAX	UNIT
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 µA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 µA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0,	I_O = 0	6 V			8		160		80	µA
C_i			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C MIN	T_A = 25°C MAX	SN54HC191 MIN	SN54HC191 MAX	SN74HC191 MIN	SN74HC191 MAX	UNIT
f_{clock}	Clock frequency		2 V		4.2		2.8		3.3	MHz
			4.5 V		21		14		17	
			6 V		24		16		19	
t_w	Pulse duration	$\overline{\text{LOAD}}$ low	2 V	120		180		150		ns
			4.5 V	24		36		30		
			6 V	21		31		26		
		CLK high or low	2 V	120		180		150		
			4.5 V	24		36		30		
			6 V	21		31		26		
t_{su}	Setup time	Data before $\overline{\text{LOAD}}$↑	2 V	150		230		188		ns
			4.5 V	30		46		38		
			6 V	25		38		32		
		$\overline{\text{CTEN}}$ before CLK↑	2 V	205		306		255		
			4.5 V	41		61		51		
			6 V	35		53		44		
		D/$\overline{\text{U}}$ before CLK↑	2 V	205		306		255		
			4.5 V	41		61		51		
			6 V	35		53		44		
		$\overline{\text{LOAD}}$ inactive before CLK↑	2 V	150		225		190		
			4.5 V	30		45		38		
			6 V	25		38		32		
t_h	Hold time	Data after $\overline{\text{LOAD}}$↑	2 V	5		5		5		ns
			4.5 V	5		5		5		
			6 V	5		5		5		
		$\overline{\text{CTEN}}$ after CLK↑	2 V	5		5		5		
			4.5 V	5		5		5		
			6 V	5		5		5		
		D/$\overline{\text{U}}$ after CLK↑	2 V	5		5		5		
			4.5 V	5		5		5		
			6 V	5		5		5		

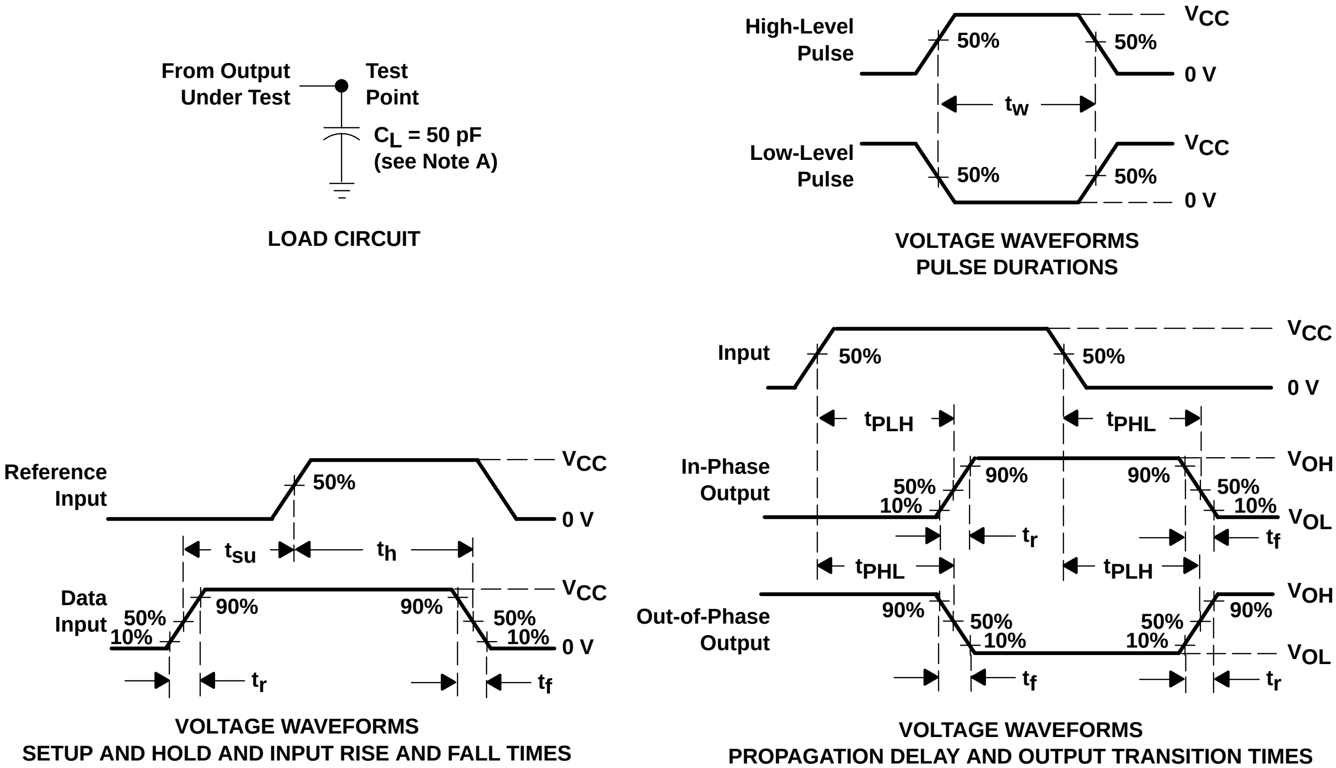
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	SN54HC191 MIN	SN54HC191 MAX	SN74HC191 MIN	SN74HC191 MAX	UNIT
f_{max}			2 V	4.2	8		2.8		3.3		MHz
			4.5 V	21	42		14		17		
			6 V	24	48		16		19		
t_{pd}	$\overline{LOAD}$	Any Q	2 V		130	264		396		330	ns
			4.5 V		40	53		79		66	
			6 V		33	45		67		56	
	A, B, C, or D	Q_A, Q_B, Q_C, or Q_D	2 V		135	240		360		300	
			4.5 V		36	48		72		60	
			6 V		30	41		61		51	
	CLK	$\overline{RCO}$	2 V		58	120		180		150	
			4.5 V		17	24		36		30	
			6 V		14	21		31		26	
		Any Q	2 V		107	192		288		240	
			4.5 V		31	38		58		48	
			6 V		26	32		49		41	
		MAX/MIN	2 V		123	252		378		315	
			4.5 V		39	50		76		63	
			6 V		32	43		65		54	
	D/$\overline{U}$	$\overline{RCO}$	2 V		102	228		342		285	
			4.5 V		29	46		68		57	
			6 V		24	38		59		49	
		MAX/MIN	2 V		86	192		288		240	
			4.5 V		24	38		58		48	
			6 V		20	32		49		41	
	$\overline{CTEN}$	$\overline{RCO}$	2 V		50	132		198		165	
			4.5 V		15	26		40		33	
			6 V		13	23		34		28	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	50	pF

PARAMETER MEASUREMENT INFORMATION



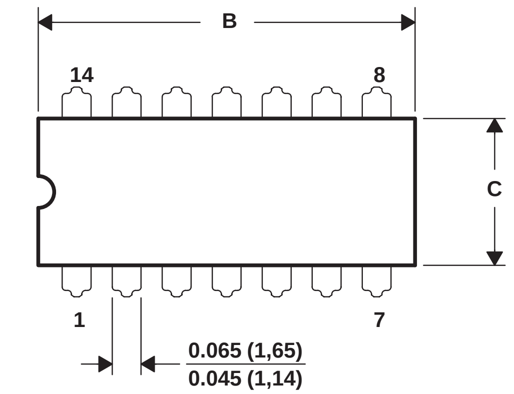
NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLH} and t_{PHL} are the same as t_{pd}.

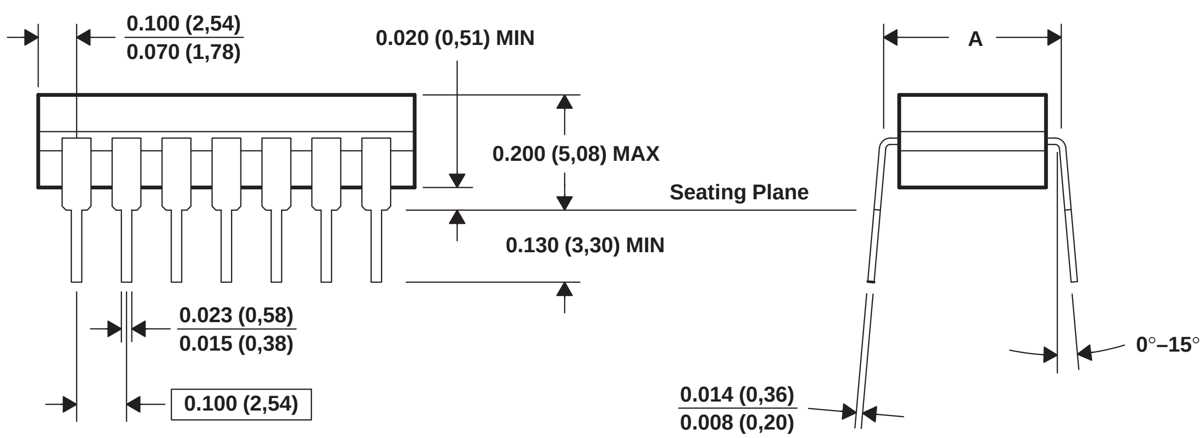
Figure 1. Load Circuit and Voltage Waveforms

J (R-GDIP-T)** **CERAMIC DUAL-IN-LINE**

14 LEADS SHOWN

PINS ** / DIM	14	16	20
A MAX	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)
A MIN	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)
B MAX	0.785 (19,94)	0.785 (19,94)	0.975 (24,77)
B MIN	0.755 (19,18)	0.755 (19,18)	0.930 (23,62)
C MAX	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)





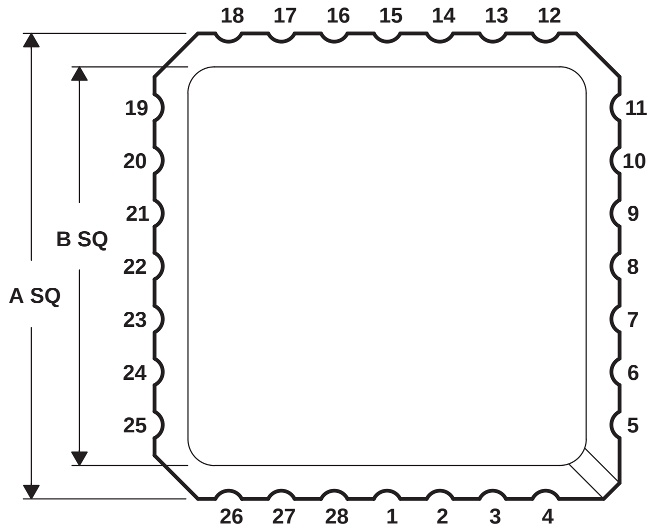
4040083/E 03/99

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, and GDIP1-T20

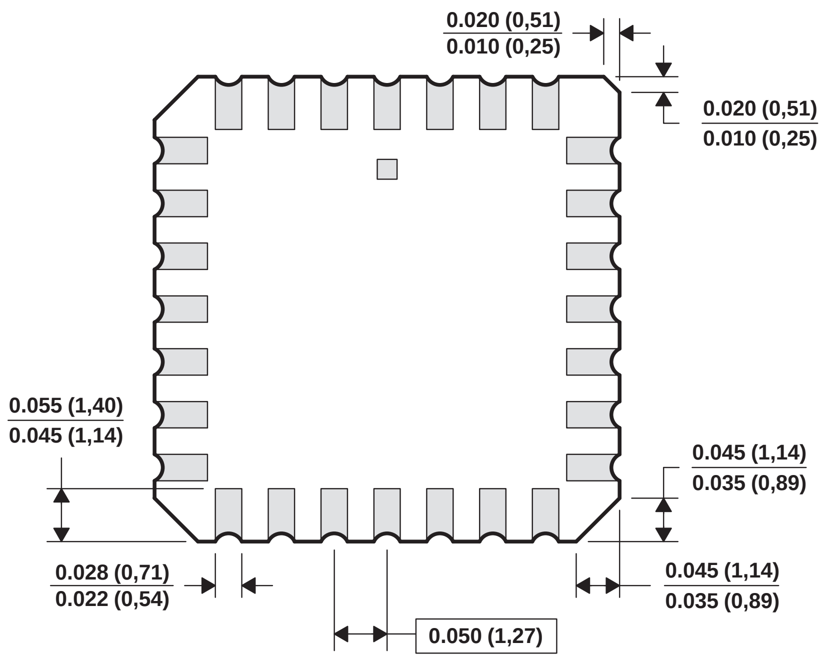
FK (S-CQCC-N**)

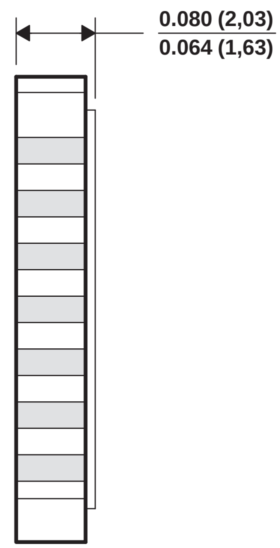
LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)





4040140/D 10/96

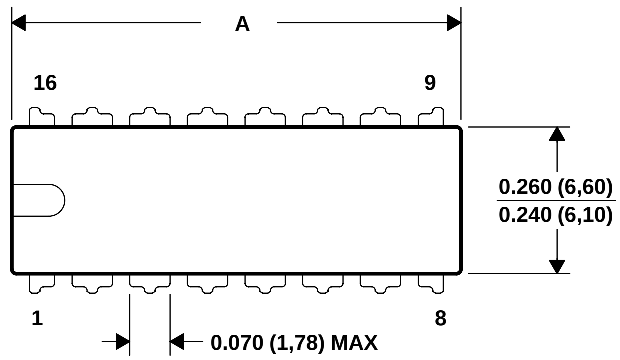
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

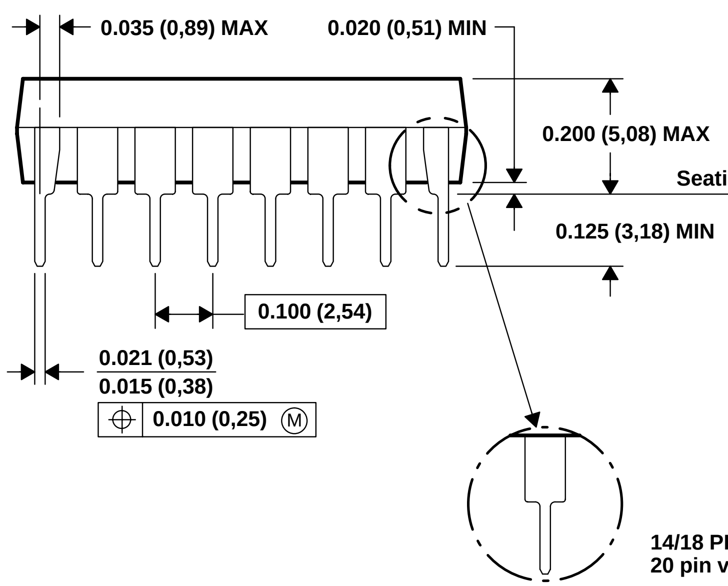
N (R-PDIP-T**)

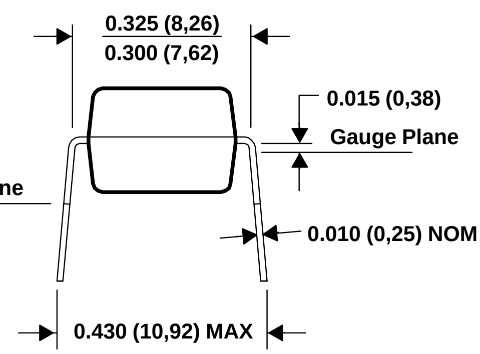
PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-100 VARIATION (C)	AA	BB	AC	AD





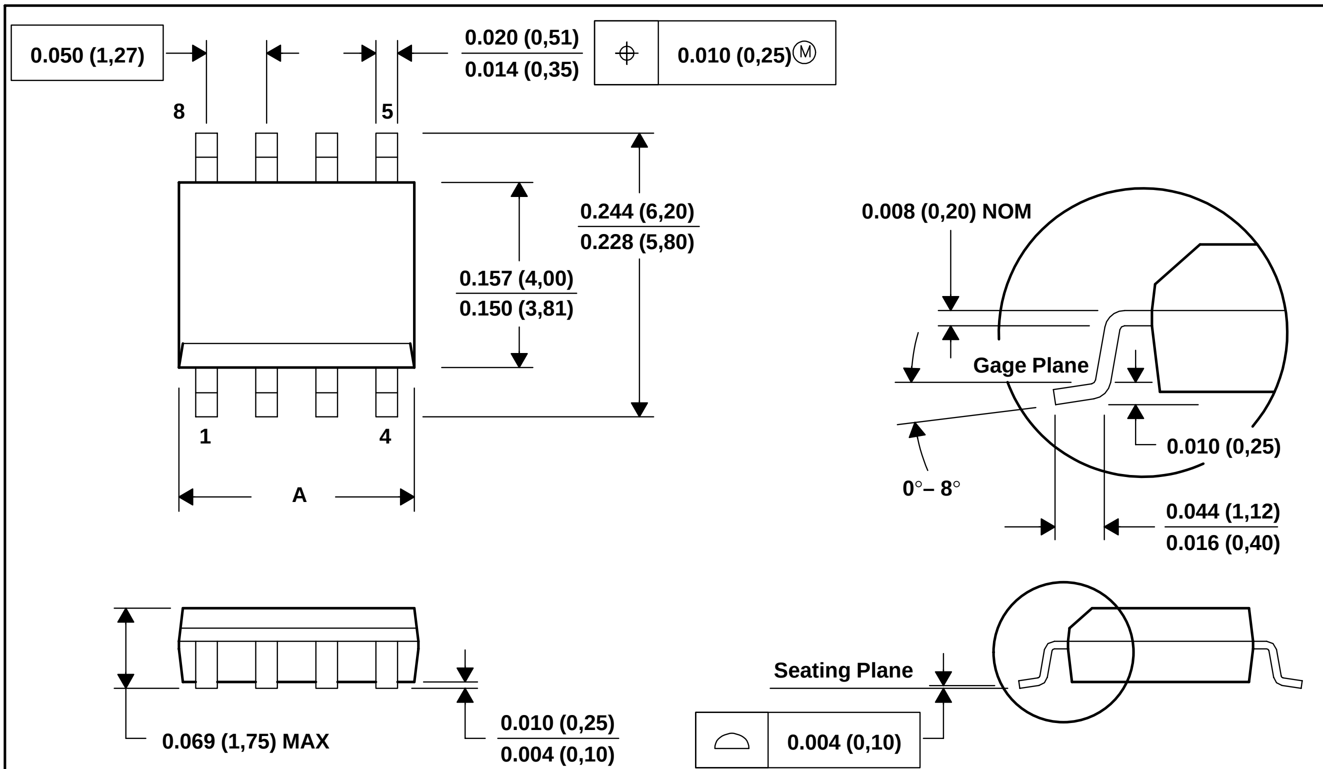


4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body lrngth (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

8 PINS SHOWN



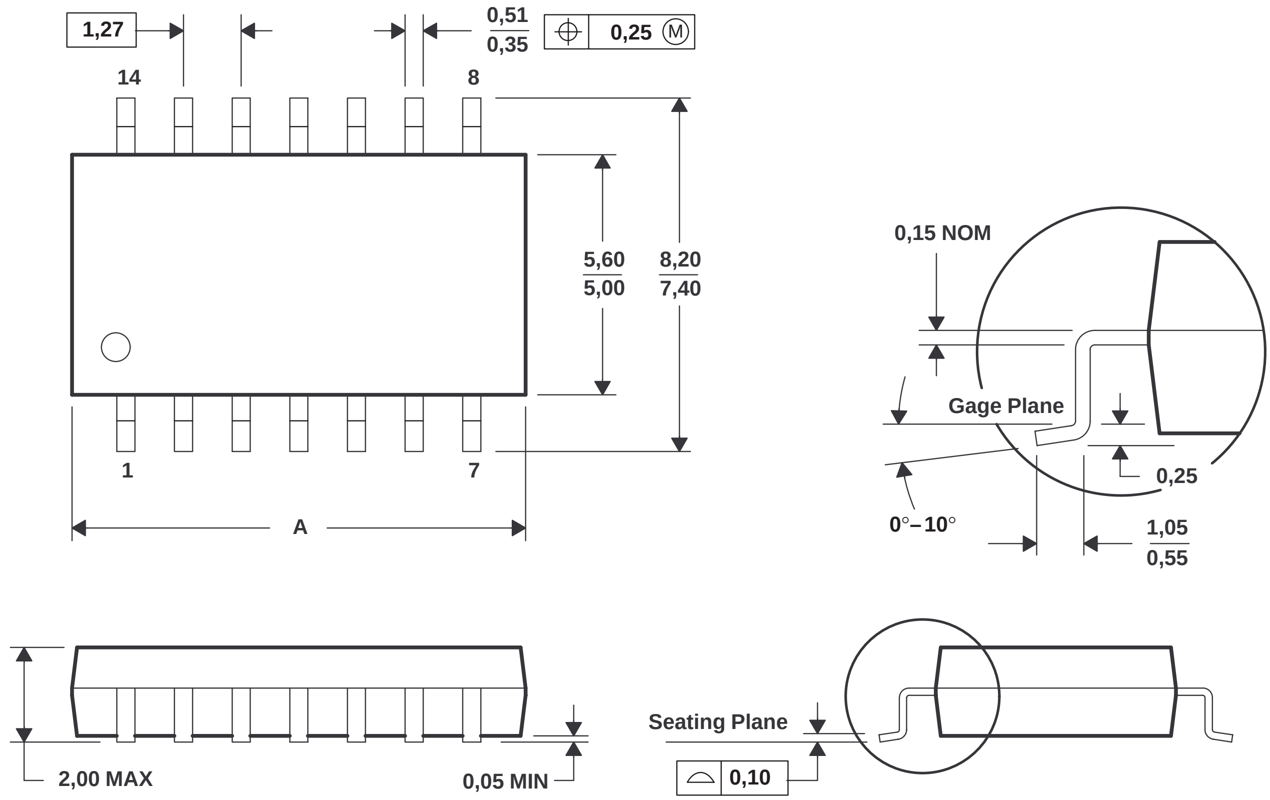
DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/E 09/01

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-012

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/B 02/95

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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